

PHD16N03LT

N-channel TrenchMOS™ logic level FET

Rev. 01 — 08 March 2004 **Product data**

1. Product profile

1.1 Description

Logic level N-channel enhancement mode field-effect transistor in a plastic package using TrenchMOS™ technology.

1.2 Features

- Logic level threshold
- Fast switching.

1.3 Applications

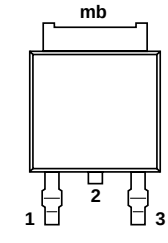
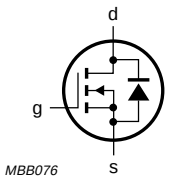
- DC-to-DC converters
- General purpose switching.

1.4 Quick reference data

- $V_{DS} \leq 30$ V
- $I_D \leq 16$ A
- $P_{tot} \leq 32.6$ W
- $R_{DSon} \leq 67$ mΩ.

2. Pinning information

Table 1: Pinning - SOT428 (D-PAK), simplified outline and symbol

Pin	Description	Simplified outline	Symbol
1	gate (g)		
2	drain (d) [1]		
3	source (s)		
mb	mounting base; connected to drain (d)		

SOT428 (D-PAK)

[1] It is not possible to make connection to pin 2 of the SOT428 package.

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3. Ordering information

Table 2: Ordering information

Type number	Package		
	Name	Description	Version
PHD16N03LT	D-PAK	Plastic single-ended surface mounted package; 3 leads (one lead cropped)	SOT428

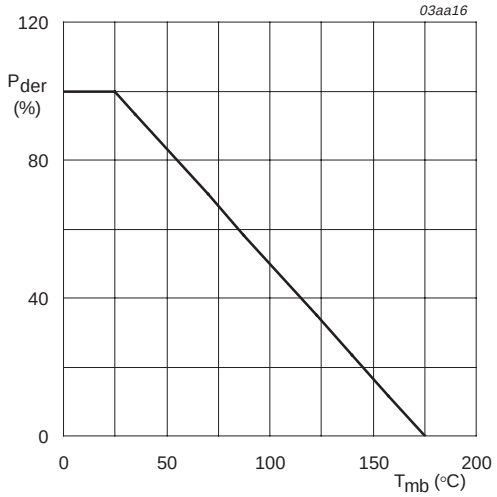
4. Limiting values

Table 3: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

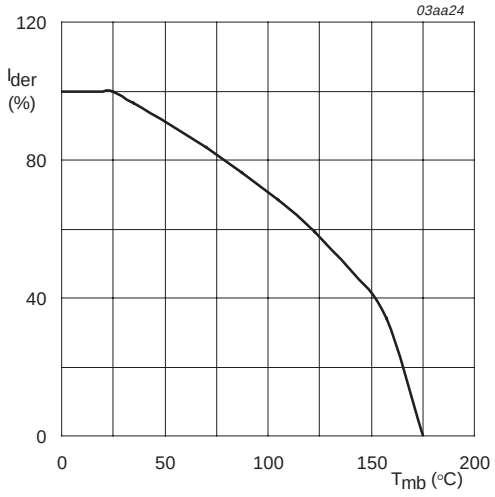
Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage (DC)	25 °C ≤ T_j ≤ 175 °C	-	30	V
V_{DGR}	drain-gate voltage (DC)	25 °C ≤ T_j ≤ 175 °C; R_{GS} = 20 kΩ	-	30	V
V_{GS}	gate-source voltage (DC)		-	±15	V
I_D	drain current (DC)	T_{mb} = 25 °C; V_{GS} = 10 V; Figure 2 and 3	-	16	A
		T_{mb} = 100 °C; V_{GS} = 10 V; Figure 2	-	11.3	A
I_{DM}	peak drain current	T_{mb} = 25 °C; pulsed; t_p ≤ 10 µs; Figure 3	-	32	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; Figure 1	-	32.6	W
T_{stg}	storage temperature		–55	+175	°C
T_j	junction temperature		–55	+175	°C
Source-drain diode					
I_S	source (diode forward) current (DC)	T_{mb} = 25 °C	-	16	A
I_{SM}	peak source (diode forward) current	T_{mb} = 25 °C; pulsed; t_p ≤ 10 µs	-	32	A

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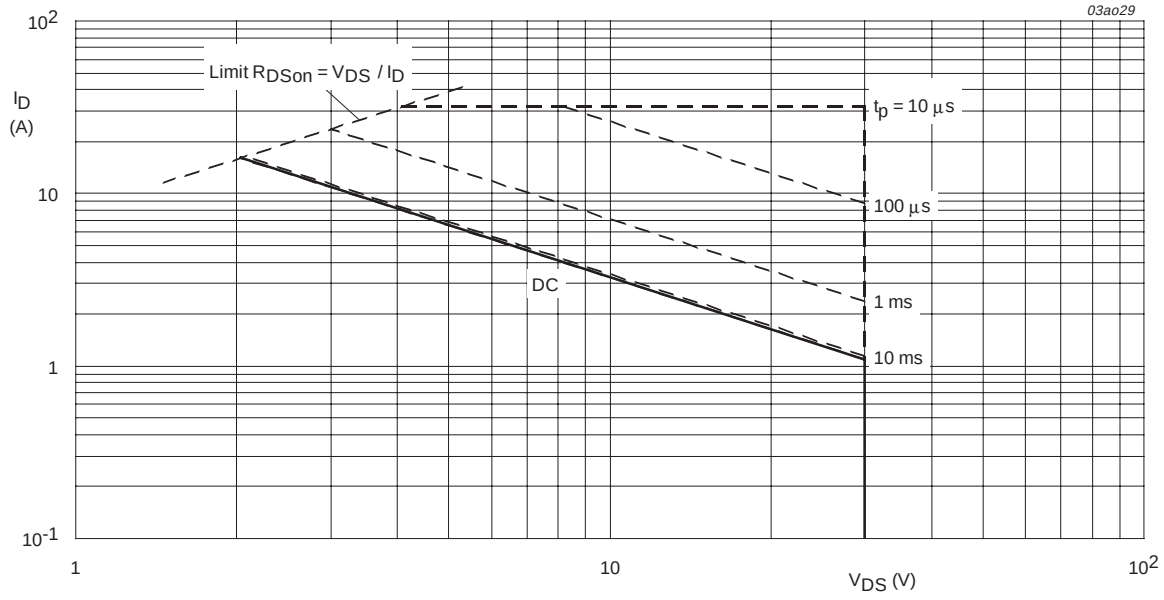
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of mounting base temperature.



$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of mounting base temperature.



T_{mb} = 25 °C; I_{DM} is single pulse; V_{GS} = 10 V

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

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5. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Figure 4	-	-	4.6	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	mounted on a printed-circuit board; vertical in still air; SOT428 minimum footprint	-	75	-	K/W
		mounted on a printed-circuit board; vertical in still air; SOT404 minimum footprint	-	50	-	K/W

5.1 Transient thermal impedance

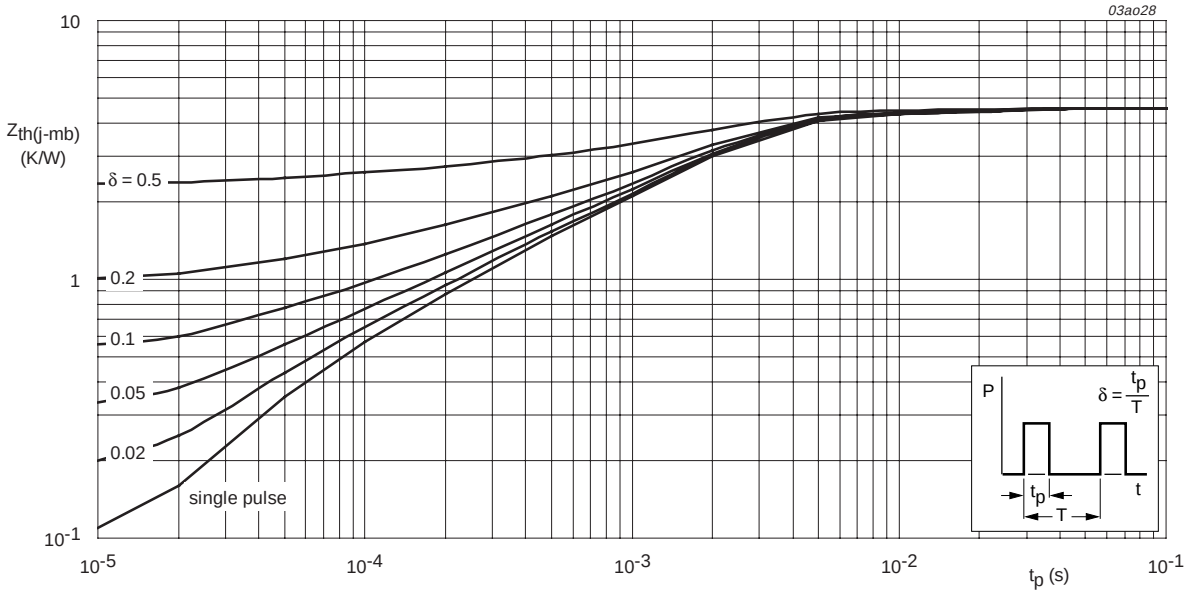


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration.

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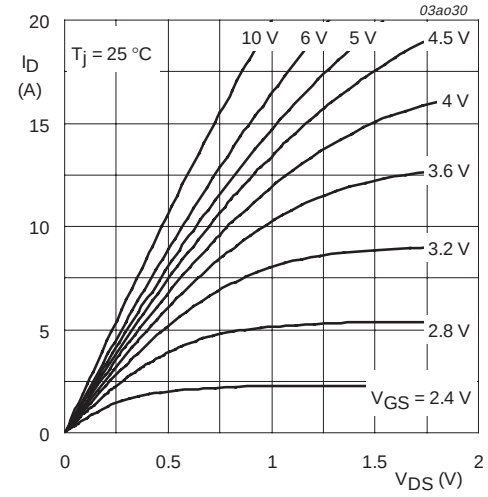
6. Characteristics

Table 5: Characteristics

T_j = 25 °C unless otherwise specified.

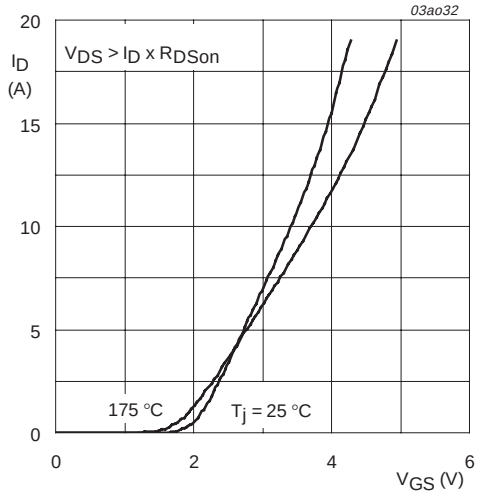
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V				
		T_j = 25 °C	30	-	-	V
		T_j = –55 °C	27	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}; Figure 9				
		T_j = 25 °C	1	1.5	2	V
		T_j = 175 °C	0.5	-	-	V
		T_j = –55 °C	-	-	2.2	V
I_{DSS}	drain-source leakage current	V_{DS} = 30 V; V_{GS} = 0 V				
		T_j = 25 °C	-	-	10	µA
		T_j = 175 °C	-	-	500	µA
I_{GSS}	gate-source leakage current	V_{GS} = ±20 V; V_{DS} = 0 V	-	2	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 16 A; Figure 7 and 8				
		T_j = 25 °C	-	50	67	mΩ
		T_j = 175 °C	-	95	127	mΩ
		V_{GS} = 4.5 V; I_D = 13 A; Figure 7	-	76	100	mΩ
Dynamic characteristics						
$Q_{g(tot)}$	total gate charge	I_D = 15 A; V_{DS} = 15 V; V_{GS} = 10 V; Figure 13	-	8.5	-	nC
Q_{gs}	gate-source charge		-	1.8	-	nC
Q_{gd}	gate-drain (Miller) charge		-	2	-	nC
C_{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = 30 V; f = 1 MHz; Figure 11	-	210	-	pF
C_{oss}	output capacitance		-	85	-	pF
C_{rss}	reverse transfer capacitance		-	60	-	pF
$t_{d(on)}$	turn-on delay time	V_{DD} = 15 V; R_L = 1 Ω; V_{GS} = 10 V; R_G = 5.6 Ω	-	8	-	ns
t_r	rise time		-	6	-	ns
$t_{d(off)}$	turn-off delay time		-	15.5	-	ns
t_f	fall time		-	5	-	ns
Source-drain diode						
V_{SD}	source-drain (diode forward) voltage	I_S = 10 A; V_{GS} = 0 V; Figure 12	-	0.98	1.2	V

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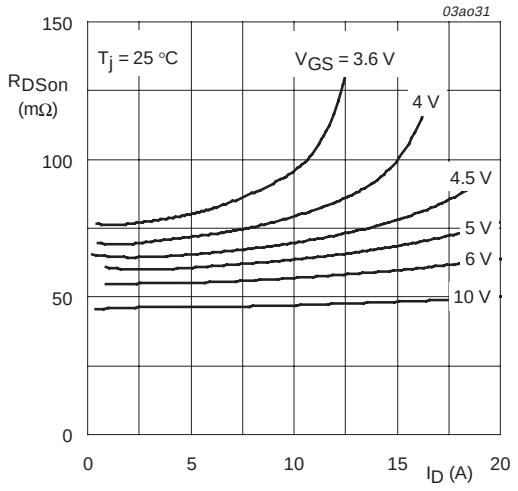
T_j = 25 °C

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.



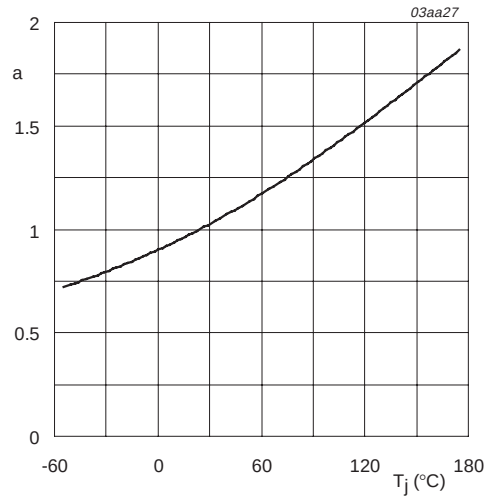
T_j = 25 °C and 175 °C; V_{DS} > I_D x R_{DSon}

Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



T_j = 25 °C

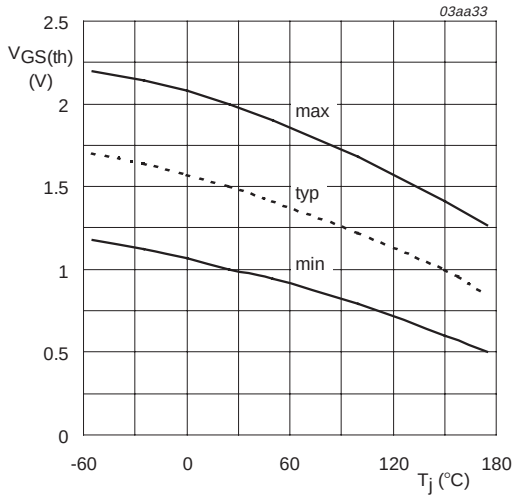
Fig 7. Drain-source on-state resistance as a function of drain current; typical values.



$$a = \frac{R_{DSon}}{R_{DSon(25^{\circ}C)}}$$

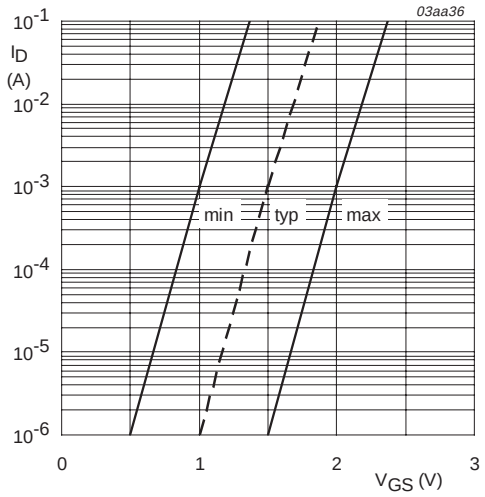
Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature.

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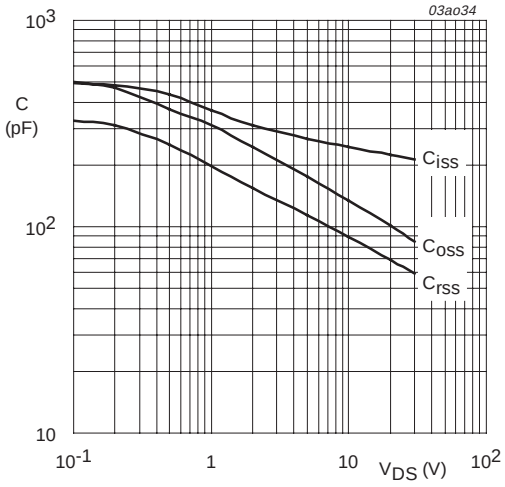
I_D = 1 mA; V_{DS} = V_{GS}

Fig 9. Gate-source threshold voltage as a function of junction temperature.



T_j = 25 °C; V_{DS} = 5 V

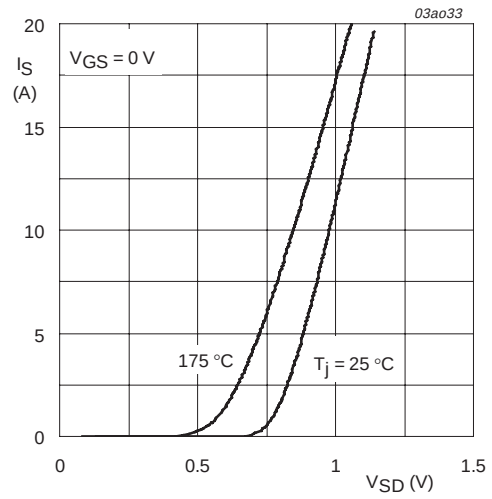
Fig 10. Sub-threshold drain current as a function of gate-source voltage.



V_{GS} = 0 V; f = 1 MHz

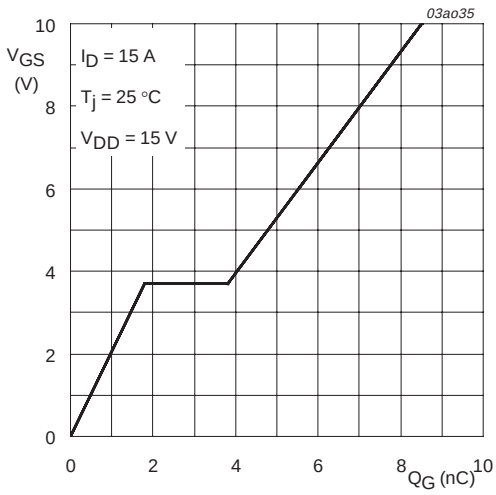
Fig 11. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.

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T_j = 25 °C and 175 °C; V_{GS} = 0 V

Fig 12. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.



I_D = 15 A; V_{DD} = 15 V

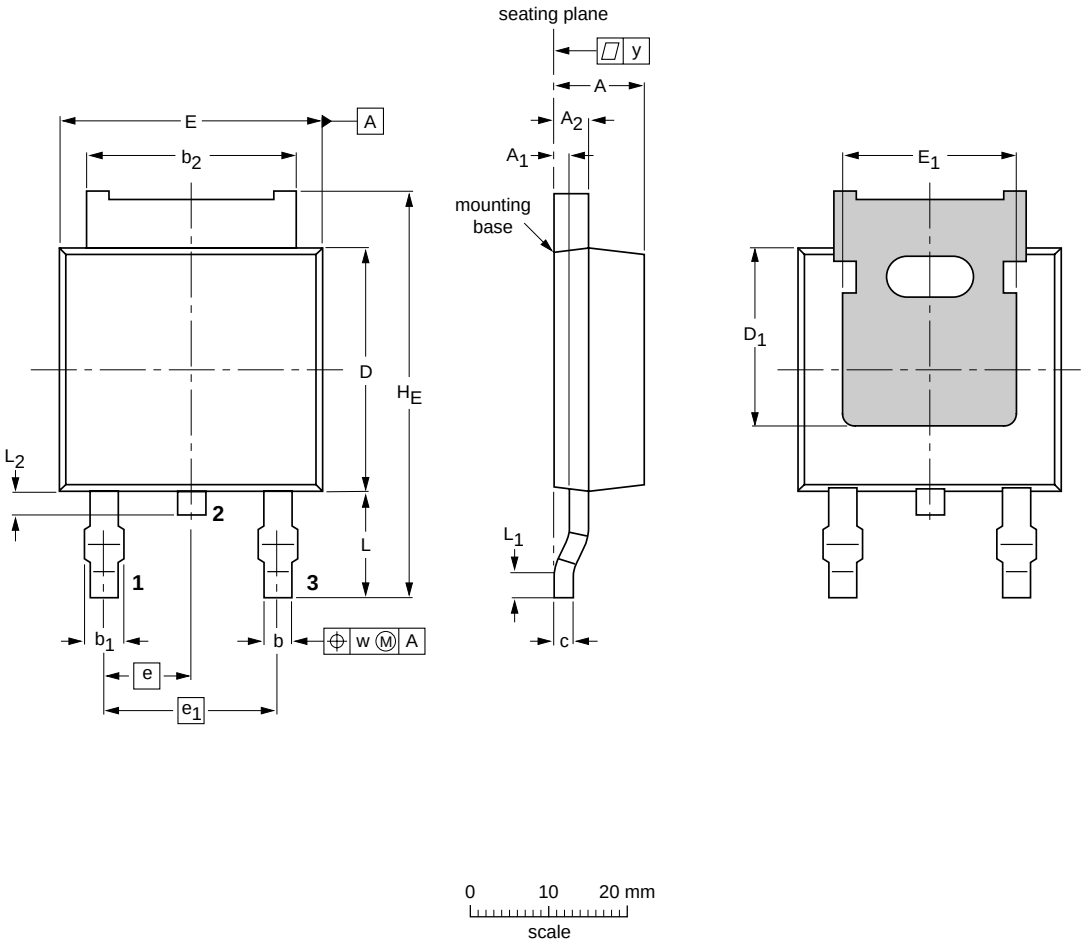
Fig 13. Gate-source voltage as a function of gate charge; typical values.

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7. Package outline

Plastic single-ended surface mounted package (Philips version of D-PAK); 3 leads (one lead cropped)

SOT428



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1 (1)	A_2	b	b_1	b_2	c	D	D_1 min.	E	E_1	e	e_1	H_E	L	L_1 min.	L_2	w	y max.
mm	2.38 2.22	0.65 0.45	0.93 0.73	0.89 0.71	1.1 0.9	5.46 5.26	0.4 0.2	6.22 5.98	4.0	6.73 6.47	4.81 4.45	2.285	4.57	10.4 9.6	2.95 2.55	0.5	0.9 0.5	0.2	0.2

Note

1. Measured from heatsink back to lead.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT428		TO-252	SC-63			~~99-09-13~~ 01-12-11

Fig 14. SOT428 (D-PAK).

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8. Revision history

Table 6: Revision history

Rev	Date	CPCN	Description
01	20040308	-	Product data (9397 750 12382).

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9. Data sheet status

Level	Data sheet status[1]	Product status[2][3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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